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### *Review of Vedic Algorithm for OFDM Applications using FIR Filter*

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#### Abstract

Digital Filter plays extremely significant role in the domain of Digital Signal Processing (DSP). Multipliers be the important apparatus of system namely, FIR filters, Microprocessors, Digital Signal Processors etc. that demands great results. The working of these application largely depends on the facts of multiplication done in lesser time. In real time multiplications the speed and power are the main criterion, therefore the quicker and power proficient multipliers are desirable. Great speed digital telecommunication systems as OFDM and DSL require real-time high-speed calculation. FFT technique be capable of reducing the number of multiplications of a FIR filter base time domain equalizer to a number of analogous to OFDM by the expenditure of delay and reception. Thus, the filter coefficients is specified with floating point data type but for execution Field Programmable Gate Array (FPGA) is use to reduce the price, area and power consumption. It is synthesized using Xilinx ISE13.1 for Spartan 3 FPGA board using Vedic multiplier and Distributive Arithmetic architectures for optimal consumption of FPGA resources.

**Keywords:** Digital FIR Filter, Vedic multiplier, Distributive Arithmetic, Urdhva Triyakbhyam (Vertically and Cross wise) Sutra, OFDM.

#### INTRODUCTION

FIR i.e. finite impulse response filter used for filtering noise from audio signals. Non-recursive filter is the other name given to FIR filter as the feedback is absent. FIR filters can be implemented digitally for any sort of frequency responses. FIR filters consist of delay, multipliers and adders to create filters output. FIR filters are much stable than the IIR filters and produces linear phase whereas IIR produces no particular phase. FIR filters are dependent on input only and consist of zeroes only. These are used for tapping of a higher order filters. No feedback therefore, non-recursive in nature. Requires less number of multipliers and adders. FIR filters has no limited cycles. FIR filter consists of zeroes only thus requires larger memory.

A CLA Adder is a fast parallel adder which reduces the propagation delay by more complex hardware which makes it costlier. The carry bits of the adder are reduced to two level logic, which is the transformation of ripple carry design. Carry look ahead adder uses the logic gates to look at the lesser order bits of the augends and addend to know whether a high order carry is to be generate or not.

Mathematics, which is derived from the Vedas, provides one step simple and fast methods and also easy ways of cross checking. It is easy to implement and learn. Vedic Mathematics with its extraordinary features has the inherent prospective to solve the mental difficulty of Mathematics - concern.

multiplication which is based upon two operations which are multiply and accumulate (MAC) are used computational arithmetic functions at present implemented.

Available multipliers are as given below which have been compared on the grounds of speed, area, and power consumption. Array multiplier: Array multiplier is simple in structure basically based upon the simple shift and add operation. In this multiplier partial products are generate by multiply the multiplicand by each one bit of multiplier. The partial product are moved according to the bit order and then finally additional at the last stage. It has some of the drawbacks like it requires large delay, power consumption and area .[2]

Booth multiplier: This multiplier reduces the quantity of partial yield generate as it scans three bits by a time are scanned reducing amount of partial yield. It also uses the encoder and selector method to decrease and reshuffle the partial products and improves the performance of multiplier. The drawback of booth multiplier is that it requires a large power consumption as it requires large number of adder cells that consumes large power. [2]

Vedic multiplier: The Vedic multiplier is based upon the urdhva triyakbhyam sutra which means vertical crosswise multiplication. This multiplier requires less area and low delay and is thus faster than any other traditional multipliers. It requires lesser area on circuit and consumes less power than any other multiplier.[2]

Thus, to get the speedy multiplication we can use Vedic multiplier. We have 16 sutras i.e. formulas in Vedic mathematics for different mathematical problems. The two sutras used for multiplication are Nikhilam navatascaramam Dasatah and Urdhava Triyagbhyam. The Nikhilam sutra is basically applied for numbers which are nearer to its bases 10, 100, 1000 which means powers of 10. It uses less power and requires mental calculations.

The one of 16 sutras which is been used for multiplication is Urdhava Triyagbhyam sutra. The Urdhava Triyagbhyam sutra is used for multiplication of large numbers. It requires less number of steps and power and easy to calculate. The Urdhava Triyagbhyam sutra (formulae) means vertical and crosswise multiplication. It is faster and requires a less computational time and power consumption than any other multipliers like booth, array, and Wallace multipliers.

Urdhava-Triyagbhyam sutra: “urdhava-triyagbhyam” that is vertical crosswise multiplication is used for Vedic multiplication. It is a general formula of multiplication. This reduces the number of multiplication steps and time and is faster multiplication formula available in Vedas. It is suitable for multiplication of larger numbers in less numbers of iterations and it also requires less power consumption.[3]

Nikhilam navatascaramam Dasatah: It is the other multiplication formula used in Vedic multiplication for numbers which are nearer to its bases like 10, 100, 1000 etc. It requires a mental calculation and limited for multiplication of larger numbers. It requires less power and less calculation steps.[3]

The other is Distributed Arithmetic (DA) [1], which change calculation of MAC to a sequence of look-up table right to use as well as sum. This declaration mainly coordinated for LUT base FPGA architectures that can be significantly grow the speed of process. Distributed arithmetic (DA) is usually meant for signal processing algorithms all over to calculate the inner effect of two vectors consist of largely of calculated results.

Modulation of a signal changes the amplitude, phase or frequency of carrier, however in OFDM only phase or amplitude or both at same time is varied but the frequency is kept constant to ensure the orthogonality among the subcarriers. The type of modulation scheme is chosen according to application. In digital modulation scheme, symbols are converted into bits; a complex number represents the number of bits to transmit according to modulation scheme employed. It is method of encoding digital data on multiple carrier frequencies. It has been developed into a wideband digital communication which is used in applications like audio broadcasting, digital television and 4G mobile communication. Advantage of using OFDM over single carrier scheme is its ability to cope up with complex equalization filters.

## LITERATURE REVIEW

In the paper [1], to implement a Digital Filter on FPGA, the major dare was to attain particular performance at smallest amount . One means to reduce the rate is to decrease the word extent. The special effects of limited word length are discuss in [1]. The special effects of with finite word length be able to reduce by choose high order filters in cascade otherwise parallel appearance. FIR filter is able of being designed by means of both windowing either optimal method. in favour of the known condition, the different method are analyse along with it is resulted that equiripple filter propose establish to be the usually right as well as optimized way to meet up the known conditions [2].

In the paper [2], Equiripple FIR filter plan process result in the filter by least order measure up to former finest as well as windowing plan method. DA architecture be able to be use for elevated speed implementations. FCSD architecture reduce the power utilization and calculation difficulty considerably [3].

In the paper [2], the complicated multiplication-accumulation procedure is transformed to the shifting and adding process as soon as the DA algorithm is straightly applied to implement FIR filter .aim to the trouble of finest configuration in the coefficient of FIR filter, the saved reserve as well as the calculative speeds, the DA algorithm is analyzed and enhanced in the form of algorithm construction, the recollection size as well as the look-up table pace. The execution of greatly proficient serial as well as parallel DA algorithm be offered. In the paper [3], It has been observed that projected Vedic multiplication is to a great extent easier than predictable. It as well show the likelihood in hardware implantation as well as display identical presentation as intellectual. For the reason of act assessment, the predictable multiplier have been synthesize, computer-generated and compare with Vedic multiplier independently as well as in FFT operation. The result shows that 80 % more hardware , memory as well as area is necessary for execution of predictable multiplier.

In the paper [4], The multiplier is mainly significant hardware block used for the application given as image processing, signal processing, everywhere where large speed multiplication are used through less power utilization. Two multipliers base on Urdhva and Nikhilam sutras from Vedic Mathematics included being implemented by a customized full adder arrangement as well as implement by means of an ASIC method in 65nm technology. The results concluded that Urdhva and Nikhilam by customized full adder be 60% and 77% faster as well as consume 37% and 50% reduced power than the array multiplier.

In the paper [5], The projected 16x16 Vedic multiplier architecture have been planned as well as synthesize by means of the Spartan 3 XC3S400 board which is being use in parallel FIR filter plan. The planned Vedic multiplier through carry select adder is compare by the alive Vedic multiplier it can be concluded that the implemented is more rapid than the active Vedic multiplier.

In 2014, M.Gnanasekaran , M. Manikandan has observed that a high speed, reduced area FIR filter is implemented using a Wallace multiplier by using a carry save adder. By using more efficient multiplier and adder will lead to a more efficient filter design with much reduced area and increased speed.[6]

In 2016, the author suggested the need of faster multiplier due to the increased constraints of delays in the DSP applications. Thus, the vedic multipliers are much faster in multiplication than the other adder due to reduction in the number of instruction steps used. The vedic multiplier along with modified adder has been implemented based upon the URDHVA TIRYAKBHAYAM sutra based upon the improved calculations.[7]

In 2015, the author compared the conventional multiplier with the efficient signed bits Vedic multiplier in terms of path delays. The Vedic multiplier is based upon the Urdhva Tiryakbhayam sutra. It has been experimented that the number of look up tables required for projected work are comparatively fewer than the conventional ones .[8]

In 2016,the author has designed Orthogonal Frequency Division Multiplexing to reduce the consequence of multipath fading by separating the frequency band into narrow sub bands to improve the fading effect and avoid inter symbol interference. In this an author proposes a filtered OFDM using window function based FIR filter. The projected FOFDM implementing with a very low band release with the same BER presentation compared to the predictable OFDM.[9]

### PROPOSED WORK

The proposed work uses vedic multiplier based FIR filter for OFDM block implemented using VHDL coding to reduce the number of multiplications for an FIR filter based time domain equalizer to a number of comparable OFDM at the cost of delay and reception. The proposed work uses Xilinx ISE13.1 and implemented on Spartan 3 FPGA board for cost reduction and less power consumption.

The FIR Filter block diagram with the vedic multiplier is as shown below for reduction in number of multiplication steps and less iterations.

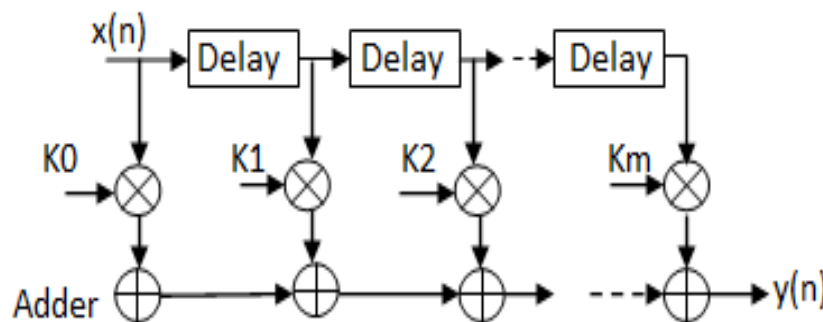


FIGURE 1. THE REALIZATION OF M-TAP FIR FILTER

Vedic multiplier as this is much fast faster than other conventional multipliers as the throughput suffers if the multiplier is not fast. Secondly, a 32 bit CLA Adder is implemented using the VHDL coding. Adders are working in combination with the multiplier in the FIR filter as the filter consists of the MAC (multiply accumulate ) unit. Thirdly, the delay unit which provides a sample signal delay to other elements. The signal flow in the filter is strictly feed forward as all the inputs are connected to the output in the forward direction.

Distributive Arithmetic: The FIR filter implementation depends on the multiply accumulate (MAC) structure. But as we know that the multipliers are the limited resources of field programmable gate array (FPGA). Therefore, the filter implementation on FPGA should be either consisting of less number of multipliers or it should be multiplier less. Thus, for this drawback we can use DA architecture which is based upon multiplier free architecture as it based on the look up tables (LUT), scaling accumulators, delay to execute FIR filter.[1]

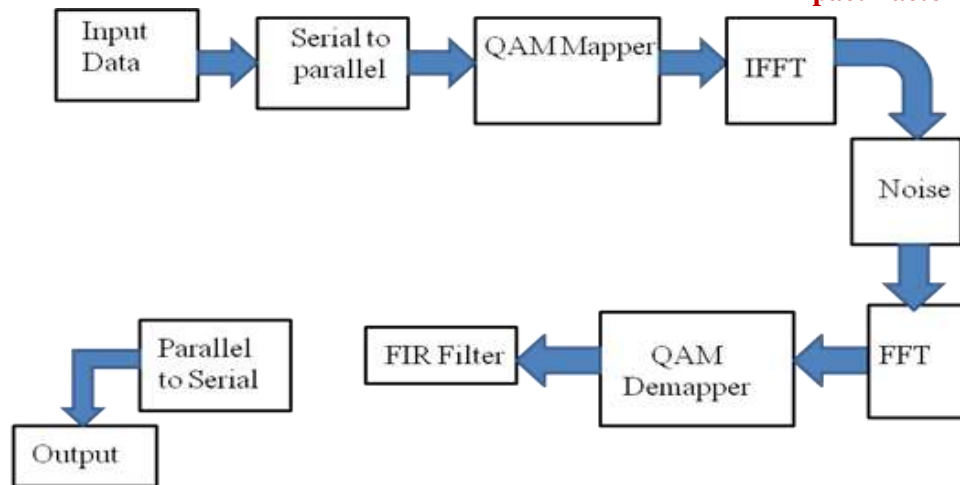


FIGURE 2 : THE PROPOSED BLOCK DIAGRAM

Modulation of a signal changes the amplitude, phase or frequency of carrier, however in OFDM only phase or amplitude or both at same time is varied but the frequency is kept constant to ensure the orthogonality among the subcarriers. The type of modulation scheme is chosen according to application. In digital modulation scheme, symbols are converted into bits; a complex number represents the number of bits to transmit according to modulation scheme employed.

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## CONCLUSION

A usual way of 32 bit floating point number multiplication is replaced by using Vedic multiplier. The researchers have implemented multipliers with different types of multipliers and the work was not applied towards any application. Important elements of Digital Signal Processing (DSP) are digital filters. Major components of digital filter are adder, multiplier and delay elements. In today's world of wireless communication the OFDM plays a vital role so to improve the speed by reducing the delay. The propose work will give a minimum order high speed, low delay, low cost and less power consumption Finite Impulse Response (FIR) digital filter which will be replaced by the conventional filter used in the OFDM with the FIR filter using the Vedic algorithm which will have less number of iterations in the Vedic multiplier than the other. Thus, improving the speed of the received output.

Its performance is confirmed using Simulink model and hardware correlated issue are handle by the Xilinx System Generator blocks. Finally, VHDL codes are generated and synthesized for OFDM architecture by means of vedic multiplier base FIR filter by means of Xilinx ISE13.1 for Spartan 3E-1200 FPGA board.

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